ADVANCE PROGRAM MINAPAD 2017

Tuesday May 16th

9h00 - 12h00 – Tutorials

Tutorial 1: ***Optical Interconnects Integration, Packaging and Reliability (S. Bernabe, L. Mendizabal, CEA-LETI)***

Tutorial 2: ***Introduction to MEMES Packaging (JP Polizzi, CEA-LETI)***

Tutorial 3: ***Reliability Analysis for Advanced Packages (Y. Ousten, IMS Bordeaux)***

Tutorial 4: ***Thermal Management in Microelectronics (JL. Diot, AssemblinoV)***

14h00 - 16h30 – Lecture - Mervi Paulasto (Aalto University, Makalu Room)
Title: Design for Reliability for Multi-Materials Assemblies

Wednesday May 17th

9h00 Welcome to MINaPAD

9h15 Opening by Jean-Luc Diot (Auditorium)

9h30: Keynote 1 ***Mervi Paulasto (Aalto University, auditorium)***
Title: : New Materials Entering MEMS

10h15 **Opening of exhibition (Exhibition Hall)**

	Session A: Emerging Applications	Session B: Flip-Chip Processes
10h45	**High Power, PCB-Embedded Inductors Based on Ferrite Powder** (C. Buttay – INSA)	**Advanced Packaging for Future Demands** (S. Lohse, FINETECH Gmbh)
11h10	**Parylene Nanostructures and Coatings for Electronics Applications** (R. Kumar, Specialty Coating Systems)	**Comparison of Low Pitch Screen Printed SAC Bumps Versus ECD Manufacturing Techniques for Power 3D Integrated Flip Chip Devices** (A. Plihon, CEA-LETI)
11h35	**A Highly Sensitive Humidity Sensor Integrated to a Flip-Chip Package for Moisture Detection in Electronics Package** (A. Quelennec, Bordeaux University)	**Qualification of electroless UBM and Wafer Level Solder Bumping for Flip Chip and WLCSP** (D. Lieske, AEMtec)
12h00-13h15	**Lunch (Exhibition Hall– Exhibition)**	

	Session C: Fan-out & 3D Packaging	Session D: Wafer Level Process
13h15	**3D and 2.5D technology: Current Adoption, Market Trends & Future Challenges** (E. Jolivet, YOLE Développement)	**Novel Method for High-Volume Via Formation in Solid-Core Glass for IC Substrates** (R. Ostholt, LPKF)
13h40	**A Wafer Level Packaging Approach for Power LEDs** (M. Volpert, CEA-LETI)	**Alternative Deposition Solution for Cost Reduction of TSV Integration** (J. Vitiello, ALTATECH)
14h05	**Application of 3D PLUS WDoD™ Technology for the Manufacturing of Electronic Modules in Implantable Products** (P. Couderc, 3D Plus)	**Substrate-less approach by single layer transfer for RFSOI performance** (A. Vinci, CEA-LETI)
14h30	**Optimization of Assembly for Fan Out Packaging** (B. Chylak, KULICKE and SOFFA)	**TSV with 40 µm Diameter Replacing Wiring Pads** (G. Parteder, AMS AG)

14h55-15h30 **Exhibition/coffee break**

	Session E: Embedded Applications / UNSETH Project	Session F: Advanced Singulation
15h30	**Technical Agenda and Building Blocks in Electronic Assembly and Packaging for Secure IoT Solutions** (B. Candaele, THALES)	**V-DOE Laser Full Cut Dicing of Thin Si IC Wafer** (J. Van Borkulo, ASMPT)
15h55	**Tamper Respondent Envelope Solutions Realized by Additive Manufacturing - Smart Packaging Solutions for Secure Applications** (F. Roscher, ENAS Fraunhofer)	**Solutions for Thin and Tiny Dies with High Die Strength and for Thinning WLCSP and eWLB Wafers** (G. Klug, DISCO HI-TEC)
16h10	**New Generation of Component Embedding Technology for High End Applications** (T. Schwarz, ATS)	**Plasma Dicing; Reducing the Cost of Singulating Thinner, Smaller die** (R. Barnett, SPTS Technologies)
16h35	**Reliability Characterization of Advanced Technological Bricks for Secure Smart Systems: HDI Embedded PCB & Anti-Tamper Solutions** (A. Lecavelier, THALES)	**Plasma Dicing on Tape** (M. Notarianni, PLASMA-THERM)
17h00	**Development of High Density Thin Wafer- Level SiP for Wafer-Level 3D Packaging and System Integration Secure Solutions in FOWLP** (A. Cardoso, NANIUM SA)	

17h30 -18h00 Exhibition 17h00 Exhibition

19h30 Social Event Restaurant « Les Jardins de Saint Cecile »

Thursday May 18th

9h00 Keynote 2 ***Christophe Zinck (ASE, auditorium)***

Title: Fan-In WLCSP a mature technology? What's next?

	Session G: Design	Session H: Advanced FC Process
9h45	**BGA Package Design Techniques for Electrical Performance Awareness** (G. Graziosi, STMicroelectronics)	**10nm CPI Study for Fine Flip Chip Attach Process and Substrate** (MC. Hsieh, STATS ChipPAC)
10h10	**Design and Verification Methodology of Heterogeneous Chips and Assemblies for Flip-Chip and 2.5D/3D Applications** (O. Guillier, CMP)	**Study of High UPH TCB Process with high throughput NCP** (H. Myodo, NAMICS Corporation)
10h35	**LGA/BGA substrate Package Design Productivity Enhancement with Cadence Ravel: DRC checks, Layout Generation & Optimization** (O. Franiatte, STMicroelectronics)	**Advanced Underfill Solutions Tailored for Next Generation Flip Chip Devices** (R. Guino, HENKEL)

11h00-11h35 Exhibition/coffee break

	Session I: High-Rel. Packaging	Session J: STD Assembly process
11h35	**Solder Paste Deposition: New Challenges for Fine Pitch Assemblies in Military Applications** (A. Chaillot, A. Mauret, MBDA)	**Large Format Packaging for IoT** (N. Fan, ASM)
12h00	**Packaging of Micro-Module Dedicated to Power Amplifier HF Application for Avionic Communication** (S. Bellenger, EOLANE Angers)	**Copper Wire in Automotive: Key Challenges and Robust Validation** (F. Quercia, STMicroelectronics)
12h25	**Hermetic Package Design and Optimization for Encapsulation of an X-Band 50 W GaN High Power Amplifier** (L. Marechal, UMS)	**Controlling Die Attach Flow - Film and Liquid Solutions** (T. Winster, HENKEL)

12h50– 14h00 Lunch & Exhibition (Exhibition hall)

	Session K Power Applications	Session L: Advanced Process & Characterization
14h00	**Development, Characterization and Optimization of Copper Clip Package for Power MOSFETs** (K.K. Lwin, UTAC)	**3D Defect Localization Technique Using Lock-in Thermography Coupled to an Automatic Test Equipment** (F. Infante, INSTRASPEC Technologies)
14h25	**Second Level Reliability of QFN Cavity Packages Based on Liquid Crystal Polymer Thermoplastics - Experimental Results and Finite Elements Analysis Comparison** (B. Levrier, BRUNO LEVRIER EXPERTISES)	**Cost effective Integration of Optical Waveguides on Thin Film Interposer** (E. Dubois, IEMN Lille)

14h50 Keynote 3 *Seung Wook Yoon (STATS-ChipPAC, auditorium)*

Title: *FO-WLP: The third Wave of Fan-Out Packaging with Scalability*

15h35 Best Paper Award

16h00 End of MINAPAD 2017